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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,824	07/10/2003	Akio Nakamura	OKI 227D2	8765

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EXAMINER	
MANDALA, VICTOR A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,824	NAKAMURA, AKIO	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22,23,25,28-30,32,35,36 and 38* is/are rejected.

7)☒ Claim(s) *24,26,27,31,33,34,37,39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 29 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner is unable to understand what the Applicant is trying to claim by the terminology found in claim 29, which states the adhesive sheet from the after the ceasing.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22, 23, 28, 30, 35, & 36 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,060,778 Jeong et al.

2. Referring to claim 22, a method of manufacturing a semiconductor device comprising: providing a wiring substrate having a substrate, (Figure 6 #32, 38, & 70), first surface and a substrate, (Figure 6 #32, 38, & 70), second surface opposed to the substrate, (Figure 6 #32, 38, & 70), first surface, the wiring substrate having a plurality of conductive lines, (Figure 6 #31a),

formed on the substrate, (Figure 6 #32, 38, & 70), first surface and a through hole, (Figure 6 area of #42), extending between the substrate, (Figure 6 #32, 38, & 70), first and second surfaces; providing a semiconductor IC chip, (Figure 6 #40), having a chip, (Figure 6 #40), first surface, a chip, (Figure 6 #40), second surface opposed to the chip, (Figure 6 #40), first surface and a plurality of chip, (Figure 6 #40), side surfaces extending between the chip, (Figure 6 #40), first and second surfaces, the semiconductor IC chip, (Figure 6 #40), including a plurality of bond pads, (Figure 6 #41), formed on the chip, (Figure 6 #40), first surface, wherein a size of the semiconductor IC chip, (Figure 6 #40), is smaller than that of the through hole, (Figure 6 area of 42); supporting the semiconductor IC chip, (Figure 6 #40), in the through hole, (Figure 6 area of #42), so that a level of the substrate, (Figure 6 #32, 38, & 70), first surface is substantially equal to a level of the chip, (Figure 6 #40), first surface; electrically connecting, (Figure 6 #39), the bond pads, (Figure 6 #41), with the conductive lines, (Figure 6 #31a), by a plurality of conductive members, (Figure 6 #39), respectively, while the supporting is maintained; coating, (Figure 6 #420), the conductive members, (Figure 6 #31a), the chip, (Figure 6 #40), first surface, the chip, (Figure 6 #40), side surfaces, the through hole, (Figure 6 area of #42), and a part of the substrate, (Figure 6 #32, 38, & 70), first surface, with a sealing resin, (Figure 6 #42), while the supporting is maintained; and ceasing the supporting of the semiconductor IC chip, (Figure 6 #40), so that the sealing resin, (Figure 6 #42), is a substantially sole member for physically connecting the semiconductor IC chip, (Figure 6 #40), with the wiring substrate, (Figure 6 #32, 38, & 70).

23. Referring to claim 23, a method of manufacturing a semiconductor device, wherein the connecting includes bonding a plurality of metal wires, (Figure 6 #39), to the bond with the conductive lines, (Figure 6 #31a).

28. Referring to claim 28, a method of manufacturing a semiconductor device comprising: providing a wiring substrate, (Figure 6 #32, 38, & 70), having a first surface and a second surface opposed to the first surface, the wiring substrate, (Figure 6 #32, 38, & 70), having a plurality of conductive lines, (Figure 6 #31a) formed on the substrate, (Figure 6 #32, 38, & 70), first surface and a through hole extending between the substrate, (Figure 6 #32, 38, & 70), first and second surfaces; putting an adhesive sheet, (Figure 6 #36), on the second surface so that the adhesive sheet, (Figure 6 #36), is exposed through the though hole, (Figure 6 area of #42); providing a semiconductor IC chip, (Figure 6 #40), having a third surface, a fourth surface opposed to the third surface and a plurality of chip, (Figure 6 #40), side surfaces extending between the third and fourth surfaces, the semiconductor IC chip, (Figure 6 #40), including a plurality of bond pads, (Figure 6 #41), formed on the third surface; positioning the semiconductor IC chip, (Figure 6 #40), on the exposed adhesive sheet, (Figure 6 #36), in the through hole, (Figure 6 area of #42); supporting the semiconductor IC chip, (Figure 6 #40), so that a level of the first surface is substantially equal to a level of the third surface of the semiconductor IC chip, (Figure 6 #40); electrically connecting the bond pads, (Figure 6 #41), of the semiconductor IC chip, (Figure 6 #40), with the conductive lines, (Figure 6 #31a), of the wiring substrate, (Figure 6 #32, 38, & 70), by a plurality of conductive members, (Figure 6 #39), while the supporting is maintained, coating, (Figure 6 #42), the conductive wires, (Figure 6 #39), the third and side surfaces, the through hole, (Figure 6 area of #42) and a part of the first surface

with a sealing resin, (Figure 6 #42), while the supporting is maintained; and ceasing the supporting of the semiconductor IC chip, (Figure 6 #40), so that the sealing resin, (Figure 6 #42), is a substantially sole member for physically connecting the semiconductor IC chip, (Figure 6 #40), with the wiring substrate, (Figure 6 #32, 38, & 70).

30. Referring to claim 30, a method of manufacturing a semiconductor device, wherein the connecting includes bonding a plurality of metal wires, (Figure 6 #39), to the bond with the conductive lines, (Figure 6 #31a).

35. Referring to claim 35, a method of manufacturing a semiconductor device comprising: providing a wiring substrate having a first surface and a second surface opposed to the first surface, the wiring substrate, (Figure 6 #32, 38, & 70), having a conductive pattern, (Figure 6 #31a), formed on the first surface and a through hole, (Figure 6 area of #42), extending from the first surface to the second surface; providing a semiconductor IC chip, (Figure 6 #40), having a third surface, a fourth surface opposed to the third surface and a plurality of side surfaces extending between the third and fourth surfaces, the semiconductor IC chip, (Figure 6 #40), including a plurality of bond pads, (Figure 6 #41), formed on the third surface, wherein a size of the chip is smaller than that of the through hole, (Figure 6 area of #42); supporting the chip, (Figure 6 #40), in the through hole, (Figure 6 area of #42), so that the first surface and third surface create a substantially flat surface; electrically connecting plurality of conductive members, (Figure 6 #39), while the supporting is maintained; the bond pads, (Figure 6 #41), with the conductive pattern, (Figure 6 #31a), by a covering, (Figure 6 #42), the conductive members, (Figure 6 #39), the third surface, the side surfaces, the through hole, (Figure 6 area of #42), and a part of the first surface, with a sealing resin, (Figure 6 #42), while the supporting is maintained,

and ceasing the supporting of the chip, (Figure 6 #40), so that the sealing resin, (Figure 6 #42), is a substantially sole member for physically connecting the chip, (Figure 6 #40), with the wiring substrate, (Figure 6 #32, 38, & 70).

36. Referring to claim 36, a method of manufacturing a semiconductor device, wherein the connecting includes bonding a plurality of metal wires, (Figure 6 #39), to the bond with the conductive lines, (Figure 6 #31a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25, 32, & 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,060,778 Jeong et al. in view of U.S. Patent No. 5,992,725 Egawa et al.

25. Referring to claims 25, 32, & 38, a method of manufacturing a semiconductor device, wherein the connecting includes applying conductive paste, (See * below), between the bond pads, (Figure 6 #41), and the conductive lines, (Figure 6 #31a), respectively.

* Jeong et al. discloses the claimed invention except for the use of a conductive paste to be used to attach the conductive wires to the bond pads and to the conductive lines of the device, but Egawa et al. does. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a conductive paste to attach a conductive wire between a

bond pad and a conductive line, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ416.

Allowable Subject Matter

Claims 24, 26, 27, 31, 33, 34, 37, 39, & 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
8/4/04

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